CLAIM AMENDMENTS

1. (Previously Amended) A transistor comprising:

a device isolation film formed on a semiconductor substrate, the device isolation film having a groove that exposes a portion of the semiconductor substrate defining an active region and having substantially vertical profile with respect to the exposed portion of the semiconductor substrate;

a gate electrode structure formed in a central portion of the active region of the semiconductor substrate and separated from the device isolation film, wherein the gate electrode structure further comprises:

a stacked structure of a gate oxide film, a first gate electrode and a second electrode,

an oxide layer formed on a side wall of the first gate electrode, and

nitride spacers formed on the oxide layer on the sidewall of the first gate electrode and on a side wall of the device isolation film;

lightly doped drain (LDD) regions formed in the active region of the semiconductor substrate on both sides of the gate electrode structure;

source/drain regions formed in the active region of the semiconductor substrate on both sides of the gate electrode structure; and

second and third insulating films filling and planarizing the space above the active region and between the gate electrode structure and the device isolation film.

2. (Previously Amended) The transistor according to claim 1, wherein , the vertical profile of the device isolation film is modified near the junction of the device isolation film and the semiconductor substrate such that the device isolation film has a substantially rounded profile.

3. (Previously Amended) The transistor according to claim 1, further comprising a hard mask layer on the gate electrode structure.

4. (Withdrawn from consideration) A method for fabricating a transistor, comprising the steps of:

forming a device isolation oxide film for defining a groove which corresponds to an active region at the upper portion of a semiconductor substrate;

forming a first gate electrode by positioning a gate oxide film in the active region;

forming a first oxide film on the surface of the first gate electrode;

forming a lightly doped drain (LDD) region in the active region at both sides of the first gate electrode;

forming an insulation film spacer at both sides of the first gate electrode and at the side walls of the device isolation film;

forming a source/drain junction region on the semiconductor substrate at both sides of the first gate electrode including the insulation film spacer;

forming second and third planarized oxide films between the first gate electrode including the first insulation film spacer and the device isolation oxide film; and

forming a gate electrode having a stacked structure of a first gate electrode, second gate electrode and hard mask layer, by forming the second gate electrode and the hard mask layer on the first gate electrode.

5. (Withdrawn from consideration) The method according to claim 4, wherein the first gate electrode and the second gate electrode comprise polysilicon.

6. (Withdrawn from consideration) The method according to claim 4, wherein the first gate electrode comprises polysilicon and further wherein the first oxide film is formed by thermally oxidizing the first gate electrode.